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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,649	12/20/2001	James C. McKinnell	10011490-1	5091

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EXAMINER

MAI, ANH D

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/029,649

Applicant(s)

MCKINNELL, JAMES C.

Examiner

Anh D. Mai

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) 18-32 and 35-59 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17, 33 and 34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/20/01.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group IA, Claims 1-17 and 33-34 in the Election filed April 5, 2004 is acknowledged.

### *Claim Objections*

2. Claims 4, 5, 13 and 14 are objected to because of the following informalities:

Claim 4, line 2 recites: "region having a **closed environment**".

Claim 5, line 2 recites: "**hermetically sealed** region".

These two terms are the same, thus, they are claiming a same subject matter.

Similar reasoning also applies to claims 13 and 14.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 and 33-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohara et al. (U.S. Patent No. 5,668,033).

With respect to claim 1, Ohara teaches an electrical device as claimed including:

first (32) and second (32) substrates, at least one having a semiconductor layer (21) thereon; and

a bond structure (24) bonding the first substrate (32) to the second substrate (33), the bond structure (24) including an alloy bonded to the semiconductor layer (21) and composed of noble metal (Au) alloyed with an oxide affinity material (e.g., Ti) having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed. (See at least first embodiment col. 3, line 29-col. 11, line 11, Figs. 1-13).

With respect to claim 2, the amount of the reducing metal (e.g., Ti) is less than that of the gold in the bonding layer (24), thus, not more than about half the weight of the alloy (24).

With respect to claim 3, the electrical device of Ohara further comprising electrical insulation (26, 29...) situated between the first (32) and second (33) substrates for electrically isolating a plurality integrated circuits. (See Fig. 8).

With respect to claims 4 and 5, the electrical device of Ohara further comprising a region having a closed environment or a hermetically sealed region between the first (32) and second (33) substrates, wherein the region is defined at least in part by the bond structure.

With respect to claim 6, the alloy bonded to the semiconductor layer (21) of Ohara is sufficient to maintain an alignment of the first substrate (32) with respect to the second substrate (33).

With respect to claims 7 and 8, since the oxide affinity material (e.g., Ti) of Ohara are reduction metal, therefore, the oxide affinity material of Ohara is inherently having a free energy

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that is lower than that of silicon dioxide and should have a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

With respect to claim 9, the alloy bonded to the semiconductor layer (21) of Ohara is composed of noble metal (Au) alloyed with a material selected from the group consisting of Al, Nb, Ti, Ta and Zr. (See col. 8, line 55).

With respect to claim 33, Ohara teaches an electrical device as claimed including: first (32) and second (33) substrates bonded together with a first material (24) having dispersed therein a reducing agent (e.g., Ti) for the diffusion therein of oxidation of a second material of which at least one of the first (32) and second (33) substrates is composed, wherein the reducing agent (e.g., Ti) has a higher affinity for oxygen than that of the second material. (See Figs. 1-13).

With respect to claim 34, the first material (24) of Ohara comprises gold and the second material comprises silicon.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohara '033 in view of Merchant et al. (U.S. Patent No. 6,118,181).

With respect to claim 10, Ohara teaches an electrical device as claimed including: first (32) and second (33) semiconductor wafers including an integrated circuits, wherein:

the first semiconductor wafer (32) has a silicon layer (21) thereon;

the silicon layer (21) on the first semiconductor wafer (32) is bonded to the second semiconductor wafer (32) by gold alloyed with an oxide affinity material (e.g., Ti) having an oxygen affinity higher than that of silicon. (See Figs. 1-13).

Thus, Ohara is shown to teach all the features of the claim with the exception of explicitly disclosing the plurality of integrated circuit on each wafers.

However, Merchant teaches bonding of first (23) and second (21) semiconductor wafers wherein each including a plurality of integrated circuits. (See Figs. 2A-E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the semiconductor wafers of Ohara wherein each wafers includes a plurality of integrated circuits as taught by Merchant to increase the amount of devices can be formed on a given area. This, wafers stacking, is well known in the art.

With respect to claim 11, the amount of the reducing metal (e.g., Ti) is less than that of the gold in the bonding layer (24), thus, not more than about half the weight of the alloy (24).

With respect to claim 12, the silicon layer (21) on the first semiconductor wafer (32) has a native oxide layer thereon. (See col. 8, ll. 53-54).

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With respect to claims 13 and 14, the electrical device of Ohara further comprising a closed environment or a hermetically sealed region between the first (32) and second (33) semiconductor wafers that is defined in part by:

the silicon layer (21) on the first semiconductor wafer (32); and

the gold alloyed with the oxide affinity material (e.g., Ti).

With respect to claim 15, Ohara teaches an electrical device as claimed including:

first (32) and second (33) semiconductor wafers one including an integrated circuits;

silicon (21) on the first semiconductor wafer (32); and

a bonding structure (24) including gold alloyed with a material (e.g., Ti) having a free energy lower than that of silicon dioxide, wherein the first semiconductor wafer (32) is bonded to the second semiconductor wafer (33) by the gold alloy that is bonded to the silicon (21) on the first semiconductor wafer (32). (See Fig. 1-13).

With respect to each wafers includes a plurality of integrated circuit, similar reasoning as that of claim 10 is also applied here.

With respect to claim 16, the free energy of the material (e.g., Ti) of Ohara is inherently less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

With respect to claim 17, the material (e.g., Ti) of Ohara selected from the group consisting of Ti, Al.

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***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,998,665 Hayashi

U.S. Patent No. 5,183,769 Rutter et al.

(U.S. Pub No. 20030183307 Liebeskind et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



A.M  
April 22, 2004